TX32M2300 Data Manual

泰芯半导体
TaiXin Semiconductor

Revision Record

Date	Version	Description
2023-02-03	V2.1	1. Solve the garbled code problem when some devices are opened for reading;
2022-08-12	V2.0	1. Reformatted the document;

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Contents

1. Product Overview

1.1. Overview

This product uses a high-performance 32-bit microcontroller with a maximum operating frequency of 72MHz, built-in 32KB high-speed Flash memory, 6KB SRAM, rich enhanced I/O ports and peripherals to connect to the external bus. This product contains 1 12-bit ADC, 1 8-bit precision DAC, 1 multi-function comparator, 3 operational amplifiers, 1 16-bit advanced timer, 5 16-bit general purpose timers, 1 32-bit general purpose timer, 1 Watchdog timer, 1 System tick timer. Also includes the standard communication interface: 2 SPI/IIC interface and 2 UART interface, among which UART0 can realize the code upgrade from any pin, built-in a 32 bit division 16 unsigned divider.

The operating voltage of this product series is 2.0V~5.5V, and the operating temperature range is -40℃ ~ 105℃. A variety of power saving operating modes ensure the requirements of low power applications.

This product is available in 4 packages, including LQFP32, SSOP28, SSOP24 and TSSOP20. The peripherals in the device are configured differently depending on the package form.

A basic introduction to all peripherals in this family is given below.

These rich peripheral configurations make this product microcontroller suitable for a variety of applications:

- Fan, fan, etc
- Consumer Electronics
- Smart home
- Motor drives and application controls
- Medical and handheld devices

- Industrial Controls
- Industrial applications: Programmable controllers (PLCS), frequency converters, printers and scanners

1.2. Product Features

➢ Kernel and System

- 32-Bit RISC architecture CPU
- Maximum working frequency: 72MHz
- Single cycle 32-bit multiplication instruction
- 32 interrupt sources, configurable 4-layer interrupt priority, support interrupt entry address Remap
- Support bitband operation
- Support double pin debugging interface

➢ Memory

- 32K Byte Flash program memory (NO EEPROM Flash), Sector erase 20000 times
- Internal 6K Byte SRAM
- Boot Loader supports on-chip Flash, supports single/dual pin UART Online User Programming (IAP)/Online System Programming (ISP)

➢ Clock, reset, and power management

- 2V to 5.5V power supply
- Power on/power off reset (POR/PDR), Programmable Voltage Monitor (PVD)
- External 1-32MHz crystal oscillator
- Factory-tuned 26MHz(+/ -1.5%) high speed oscillator embedded
- Embedded 128KHz low speed oscillator
- PLL outputs 72MHz clock
- Built-in Clock Security System (CSS)

- WDT reset

- **DMA support**
  - Supported peripherals: EFLASH, UART, SPI/I2C, CRC, TIMER, ADC
- **GPIO**
  - Supports up to 30 GPIOs
  - All I/O ports can trigger edge or level response interrupts to wake up low power mode
  - All ports can input and output 5V signals
  - Support for key detection
- **Communication interface peripherals**
  - 2 SPI high-speed serial interface, Master under the maximum support system clock frequency half transmission, support 1/2/4 line master-slave mode, support I2C mode
  - 2 UART interface, support RS232/RS485 protocol, UART0 can support any IO program upgrade
- **Timer**
  - 1 16-bit advanced timer that supports 4 pairs of complementary outputs or 8 independent PWM outputs, supports dead zone insertion and event brake functions, and supports monopulse mode
  - 5 16-bit universal timers, 1 32-bit timer, each with capture function
  - 1 watchdog timer
  - 1 system tick timer
- **Hardware acceleration unit**
  - Hardware signed divider (32bit/16bit)
- **High security**
  - Support 5/7/8/16/32 bit CRC validation to ensure data accuracy
  - Support code scrambling and hardware encryption and decryption

- Low power consumption
  - Supports IDLE, STOP, and SLEEP low-power modes
  - Static power consumption <20uA@25 ° C
  - Low power wake-up time 10us fastest
- 1 12-bit high speed analog-to-digital converter
  - Supports up to 1.2Mhz sampling rate
  - Up to 10 input channels
- 1 comparator
  - Supports 7 positive end inputs and 3 negative end inputs
  - Support hardware channel polling
- 3 operational amPs
  - An op-amp in the same direction
  - Built-in 4/6/8/10/12x gain available
  - Closed-loop gain bandwidth optional
- Built-in temperature sensor
- High reliability
  - ESD HBM 8KV
  - EFT ±4500V
  - Latch-up ±100mA @105℃
- 96-bit chip Unique ID (UID)
- Package
  - Die Form
  - LQFP32/SSOP28/SSOP24/TSSOP20
- Industrial grade temperature range
  - -40℃ ~ 105℃
- Apply
  - Fan, etc.

- Motor drive and application control
- Medical and handheld devices
- PC gaming peripherals and GPS platforms
- Industrial applications: Programmable controllers (PLCS), frequency converters, printers and scanners
- Alarm systems, video intercom, and heating ventilation and air conditioning systems

1.3. Pin assignment

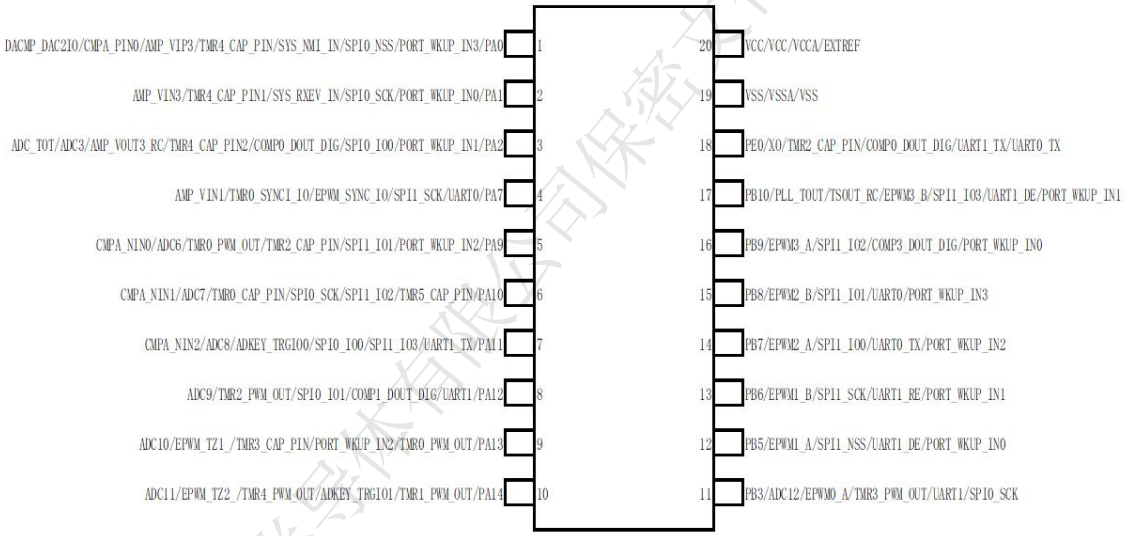


Figure 1-1 Pin package of the TX32M2300TS20 (TSSOP20)

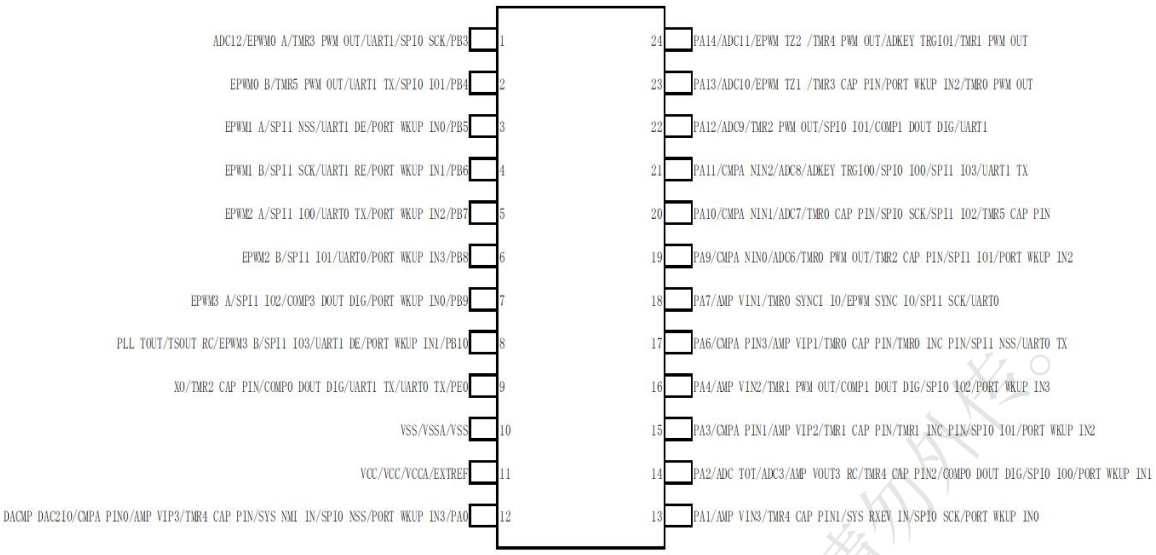


Figure 1-2 TX32M2300SS24 (SSOP24) pin package diagram

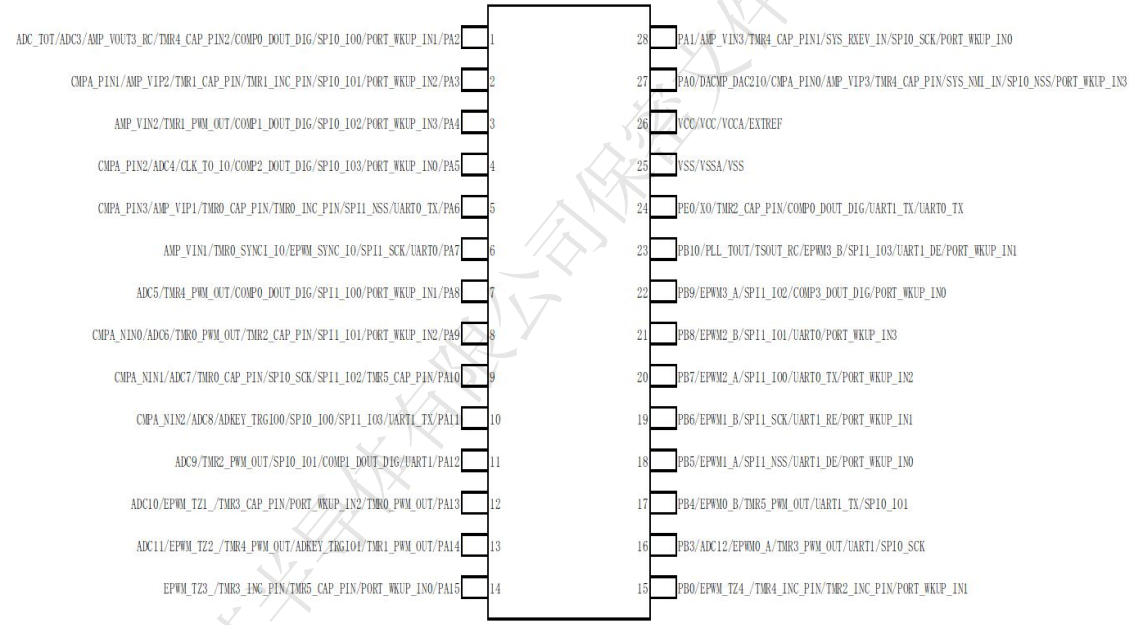


Figure 1-3 Pin package of the TX32M2300SS28 (SSOP28)

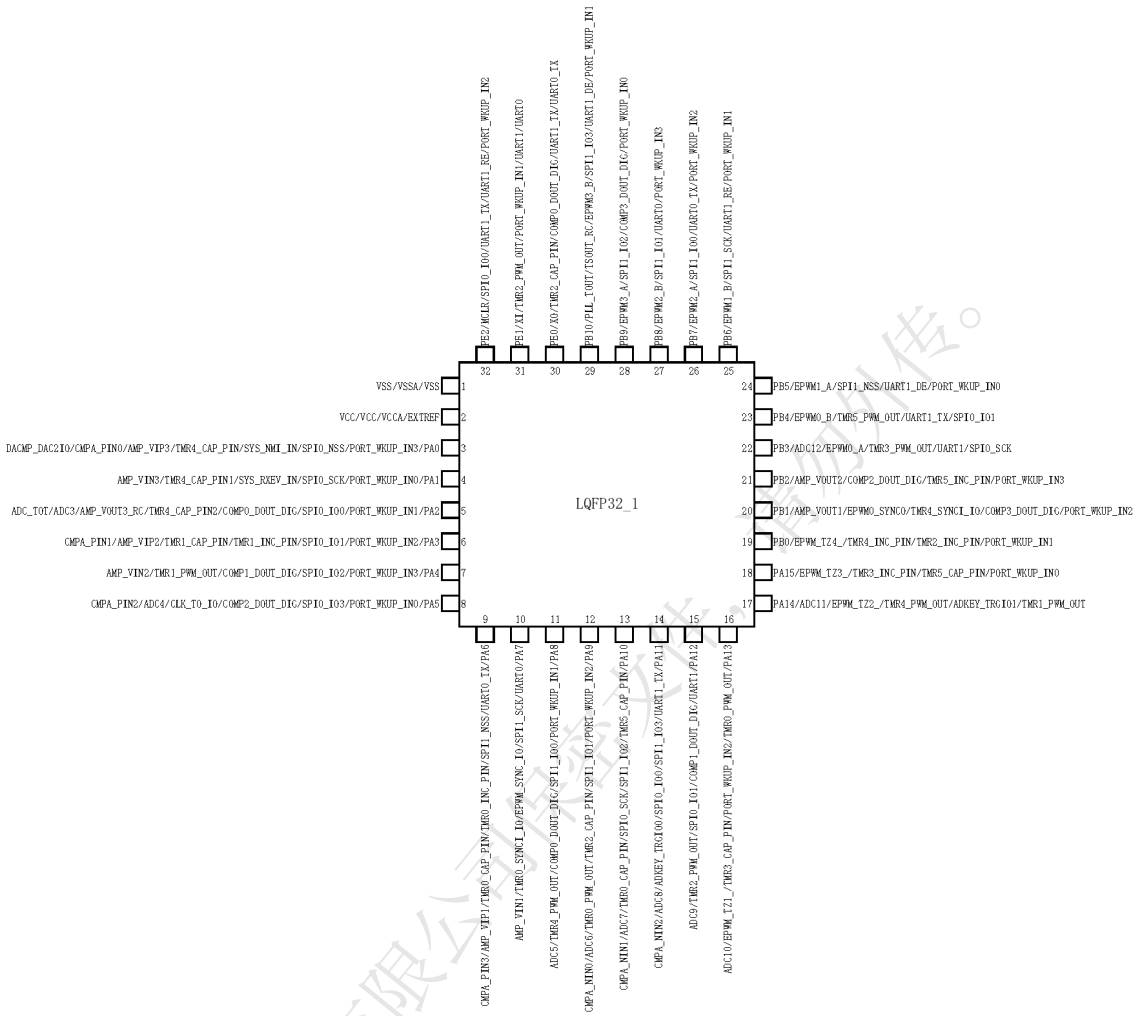


Figure 1-4 Pin package of the TX32M2300LQ32 (LQFP32)

1.4. Pin Definition

Table 1-1 Pin definitions

Encapsulation				Pin name	Function description of the pin	
SSOP20	SSOP24	SSOP28	LQFP32		Multifunctional (Alternate) Functions)	Other functions
19	10	25	1	VSS		-
20	11	26	2	VCC		-
1	12	27	3	PA0	MCO UART0_UP0, TMR4_CAP, SYS_NMI,	DAC CMPA_PIN0 AMP_VIP3

					SPI0_NSS, WKUP3	
2	13	28	4	PA1	UART0_UP1, TMR4_CAP1, SYS_REV, SPI0_SCK WKUP0	AMP_VIN3
3	14	1	5	PA2	UART0_UP2, TMR4_CAP2, COMP0_OUT0, SPI0_DAT0 WKUP1	ADC3, AMP_VOUT3
-	15	2	6	PA3	UART0_UP3, TMR1_CAP, TMR1_INC, SPI0_DAT1, WKUP2	CMPA_PIN1, AMP_VIP2
-	16	3	7	PA4	UART0_UP4, TMR1_PWM, COMP0_OUT1, SPI0_DAT2, WKUP3	AMP_VIN2
-	-	4	8	PA5	UART0_UP5, MCO, COMP0_OUT2, SPI0_DAT3, WKUP0	ADC4 CMPA_PIN2
-	17	5	9	PA6	UART0_UP6, TMR0_CAP, TMR0_INC, SPI1_NSS, UART0_TX	CMPA_PIN3, AMP_VIP1
4	18	6	10	PA7	UART0_UP7, TMR0_SYNCI, EPWM_SYNC, SPI1_SCK, UART0_RX	AMP_VIN1
-	-	7	11	PA8	UART0_UP8, TMR4_PWM, COMP0_OUT0 SPI1_DAT0, WKUP1	ADC5
5	19	8	12	PA9	UART0_UP9, TMR0_PWM, TMR2_CAP, SPI1_DAT1,	ADC6, CMPA_NIN0

					WKUP2	
6	20	9	13	PA10	UART0_UP10, TMR0_CAP, SPI0_SCK, SPI1_DAT2, TMR5_CAP	ADC7, CMPA_NIN1
7	21	10	14	PA11	SWD_CLK, UART0_UP11, ADC_TRIG0, SPI0_DAT0, SPI1_DAT3, UART1_TX	ADC8, CMPA_NIN2
8	22	11	15	PA12	SWD_DAT UART0_UP12, TMR2_PWM, SPI0_DAT1, COMP0_OUT1, UART1_RX	ADC9
9	23	12	16	PA13	SWD_CLK, UART0_UP13, EPWM_TZ1_, TMR3_CAP, WKUP2, TMR0_PWM	ADC10
10	24	13	17	PA14	SWD_DAT, UART0_UP14, EPWM_TZ2_, TMR4_PWM, ADKEY_TRIG1, TMR1_PWM	ADC11
-	-	14	18	PA15	UART0_UP15, EPWM_TZ3_, TMR3_INC, TMR5_CAP, WKUP0	-
-	-	15	19	PB0	UART0_UP16, EPWM_TZ4_, TMR4_INC, TMR2_INC, WKUP1	-
-	-	-	20	PB1	UART0_UP17, EPWM_SYNC0, TMR4_SYNCI, COMP0_OUT3, WKUP2	AMP_VOUT1
-	-	-	21	PB2	UART0_UP18,	AMP_VOUT2

					COMP0_OUT2, TMR5_INC, WKUP3	
11	1	16	22	PB3	UART0_UP19, EPWM0_A, TMR3_PWM, UART1_RX, SPI0_SCK	ADC12
-	2	17	23	PB4	UART0_UP20, EPWM0_B, TMR5_PWM, UART1_TX, SPI0_DAT1	-
12	3	18	24	PB5	UART0_UP21, EPWM1_A, SPI1_NSS UART1_DE, WKUP0	-
13	4	19	25	PB6	UART0_UP22, EPWM1_B, SPI1_SCK, UART1_RE, WKUP1	-
14	5	20	26	PB7	UART0_UP23, EPWM2_A, SPI1_DAT0, UART0_TX, WKUP2	-
15	6	21	27	PB8	UART0_UP24, EPWM2_B, SPI1_DAT1, UART0_RX, WKUP3	-
16	7	22	28	PB9	UART0_UP25, EPWM3_A, SPI1_DAT2, COMP0_OUT3, WKUP0	
17	8	23	29	PB10	UART0_UP26, EPWM3_B, SPI1_DAT3, UART1_DE, WKUP1	-
-	-	-	30	PE0	UART0_UP27, TMR2_CAP, COMP0_OUT0,	XOSC0

					UART1_TX, UART0_TX	
-	-	-	31	PE1	UART0_UP28, TMR2_PWM, WKUP1, UART1_RX, UART0_RX	XOSCI
18	9	24	32	PE2	MCLR, UART0_UP29, SPI0_DAT0, UART1_TX, UART1_RE, WKUP2	-

Table 1-2 Port function Multiplexing AF0-AF3

Port		AF0	AF1	AF2	AF3
PA	PA0	TMR4_CAP	SYS_NMI	SPI0_NSS	WKUP3
	PA1	TMR4_CAP1	SYS_REV	SPI0_SCK	WKUP0
	PA2	TMR4_CAP2	COMP0_OUT0	SPI0_DAT0	WKUP1
	PA3	TMR1_CAP	TMR1_INC	SPI0_DAT1	WKUP2
	PA4	TMR1_PWM	COMP0_OUT1	SPI0_DAT2	WKUP3
	PA5	MCO	COMP0_OUT2	SPI0_DAT3	WKUP0
	PA6	TMR0_CAP	TMR0_INC	SPI1_NSS	UART0_TX
	PA7	TMR0_SYNCI	EPWM_SYNC	SPI1_SCK	UART0_RX
	PA8	TMR4_PWM	COMP0_OUT0	SPI1_DAT0	WKUP1
	PA9	TMR0_PWM	TMR2_CAP	SPI1_DAT1	WKUP2
	PA10	TMR0_CAP	SPI0_SCK	SPI1_DAT2	TMR5_CAP
	PA11	ADC_TRIG0	SPI0_DAT0	SPI1_DAT3	UART1_TX
	PA12	TMR2_PWM	SPI0_DAT1	COMP0_OUT1	UART1_RX
	PA13	EPWM_TZ1_	TMR3_CAP	WKUP2	TMR0_PWM
	PA14	EPWM_TZ2_	TMR4_PWM	ADKEY_TRIG1	TMR1_PWM
	PA15	EPWM_TZ3_	TMR3_INC	TMR5_CAP	WKUP0
PB	PB0	EPWM_TZ4_	TMR4_INC	TMR2_INC	WKUP1
	PB1	EPWM_SYNC0	TMR4_SYNCI	COMP0_OUT3	WKUP2
	PB2	COMP0_OUT2	TMR5_INC	-	WKUP3
	PB3	EPWM0_A	TMR3_PWM	UART1_RX	SPI0_SCK
	PB4	EPWM0_B	TMR5_PWM	UART1_TX	SPI0_DAT1
	PB5	EPWM1_A	SPI1_NSS	UART1_DE	WKUP0
	PB6	EPWM1_B	SPI1_SCK	UART1_RE	WKUP1
	PB7	EPWM2_A	SPI1_DAT0	UART0_TX	WKUP2
	PB8	EPWM2_B	SPI1_DAT1	UART0_RX	WKUP3
	PB9	EPWM3_A	SPI1_DAT2	COMP0_OUT3	WKUP0
	PB10	EPWM3_B	SPI1_DAT3	UART1_DE	WKUP1
PE	PE0	TMR2_CAP	COMP0_OUT0	UART1_TX	UART0_TX

	PE1	TMR2_PWM	WKUP1	UART1_RX	UART0_RX
	PE2	SPI0_DAT0	UART1_TX	UART1_RE	WKUP2

Table 1-3 Pin mapping table for TMR0

Peripheral	Port	
TMR0_CAP_PIN	PA6	PA10
TMR0_INC_PIN	PA6	-
TMR0_SYNCI_IO	PA7	-
TMR0_PWM_OUT	PA9	PA13

Table 1-4 Pin mapping table for TMR1

Peripheral	Port	
TMR1_CAP_PIN	PA3	-
TMR1_INC_PIN	PA3	-
TMR1_PWM_OUT	PA4	PA14

Table 1-5 Pin mapping table for TMR2

Peripheral	Port	
TMR2_CAP_PIN	PA9	PE0
TMR2_PWM_OUT	PA12	PE1
TMR2_INC_PIN	PB0	-

Table 1-6 Pin mapping table for TMR3

Peripheral	Port
TMR3_CAP_PIN	PA13
TMR3_INC_PIN	PA15
TMR3_PWM_OUT	PB3

Table 1-7 Pin mapping table for TMR4

Peripheral	Port	
TMR4_CAP_PIN	PA0	-
TMR4_CAP_PIN1	PA1	-
TMR4_CAP_PIN2	PA2	-
TMR4_PWM_OUT	PA8	PA14
TMR4_INC_PIN	PB0	-
TMR4_SYNCI_IO	PB1	-

Table 1-8 Pin mapping table for TMR5

Peripheral	Port	
TMR5_CAP_PIN	PA10	PA15
TMR5_INC_PIN	PB2	-
TMR5_PWM_OUT	PB4	-

Table 1-9 Pin mapping table for EPWM

Peripheral	Port
EPWM_SYNC_IO	PA7
EPWM_TZ1_	PA13
EPWM_TZ2_	PA14
EPWM_TZ3_	PA15
EPWM_TZ4_	PB0
EPWM0_SYNCO	PB1
EPWM0_A	PB3
EPWM0_B	PB4
EPWM1_A	PB5
EPWM1_B	PB6
EPWM2_A	PB7
EPWM2_B	PB8
EPWM3_A	PB9
EPWM3_B	PB10

Table 1-10 Pin-mapping table for the System

Peripheral	Port
SYS_NMI_IN	PA0
SYS_RXEV_IN	PA1

Table 1-11 Pin mapping table for Clock

Peripheral	Port
CLK_TO_IO	PA5

Table 1-12 Pin mapping table for Wakeup

Peripheral	Port					
PORT_WKUP_IN0	PA1	PA5	PA15	PB5	PB9	-
PORT_WKUP_IN1	PA2	PA8	PB0	PB6	PB10	PE1
PORT_WKUP_IN2	PA3	PA9	PA13	PB1	PB7	PE2
PORT_WKUP_IN3	PA0	PA4	PB2	PB8	-	-

Table 1-13 Pin mapping table for UART0

Peripheral	Port		
UART0_TX	PA6	PB7	PE0
UART0	PA7	PB8	PE1

Table 1-14 Pin mapping table of UART1

Peripheral	Port			
UART1_TX	PA11	PB4	PE0	PE2
UART1	PA12	PB3	PE1	-
UART1_DE	PB5	PB10	-	-

UART1_RE	PB6	PE2	-	-

Table 1-15 Pin mapping table for SPI0

Peripheral	Port		
SPI0_NSS	PA0	-	-
SPI0_SCK	PA1	PA10	PB3
SPI0_IO0	PA2	PA11	PE2
SPI0_IO1	PA3	PA12	PB4
SPI0_IO2	PA4	-	-
SPI0_IO3	PA5	-	-

Table 1-16 Pin mapping table for SPI1

Peripheral	Port	
SPI1_NSS	PA6	PB5
SPI1_SCK	PA7	PB6
SPI1_IO0	PA8	PB7
SPI1_IO1	PA9	PB8
SPI1_IO2	PA10	PB9
SPI1_IO3	PA11	PB10

Table 1-17 Pin mapping table for IIC0

Peripheral	Port		
IIC_SCL	PA1	PA3	PA10
IIC_SDA	PA2	PA11	PE2

Table 1-18 Pin mapping table for IIC1

Peripheral	Port		
IIC_SCL	PA7	PB6	-
IIC_SDA	PA8	PB7	-

Table 1-19 Pin mapping table for COMP0

Peripheral	Port		
COMP0_DOUT_DIG	PA2	PA8	PE0

Table 1-20 Pin-mapping table for COMP1

Peripheral	Port	
COMP1_DOUT_DIG	PA4	PA12

Table 1-21 Pin-mapping table for COMP2

Peripheral	Port	
COMP2_DOUT_DIG	PA5	PB2

Table 1-22 pin-mapping table for COMP3

Peripheral	Port	
COMP3_DOUT_DIG	PB1	PB9

Table 1-23 Pin mapping table for ADKeys

Peripheral	Port
ADKEY_TRGI00	PA11
ADKEY_TRGI01	PA14

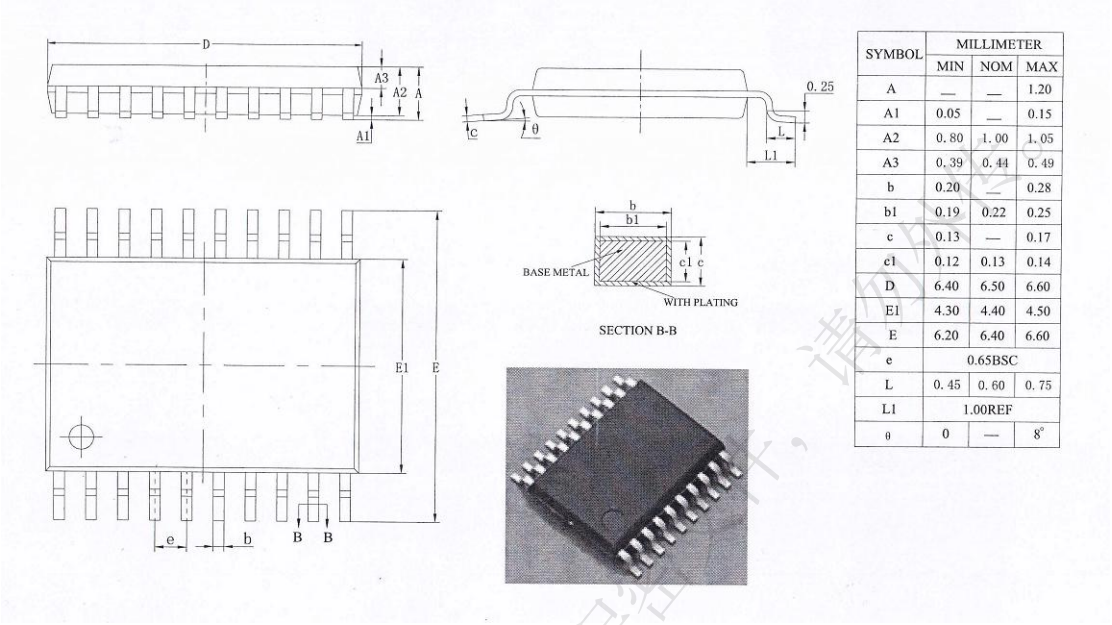
1.5. Encapsulating information

The models of the TX32M2300 series are as follows:

Model number	encapsulation	Packaging
TX32M2300TS20	TSSOP20	Tube mount
TX32M2300SS24	SSOP24	Tube mount
TX32M2300SS28	SSOP28	Tube mount
TX32M2300LQ32	LQFP32	Disc mount

1.6. Package size diagram

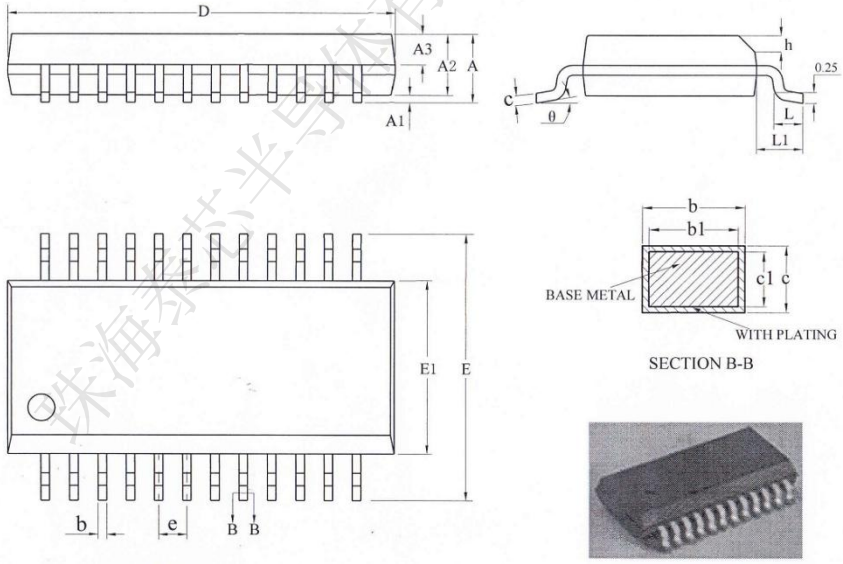
1.6.1. TSSOP20



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.80	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	—	0.28
b1	0.19	0.22	0.25
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	6.40	6.50	6.60
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00REF		
θ	0	—	8°

Figure 15 TSSOP20 - package POD diagram

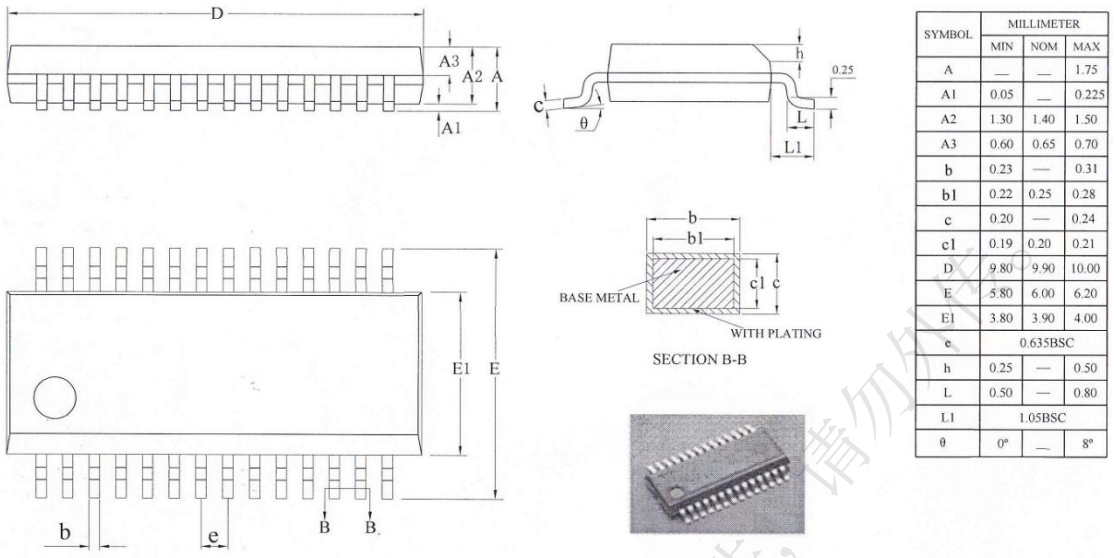
1.6.2. SSOP24



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	0.15	0.25
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.23	—	0.31
b1	0.22	0.25	0.28
c	0.20	—	0.24
c1	0.19	0.20	0.21
D	8.55	8.65	8.75
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	0.635BSC		
h	0.30	—	0.50
L	0.50	—	0.80
L1	1.05REF		
θ	0	—	8°

Figure 16 SSOP24 - package POD diagram

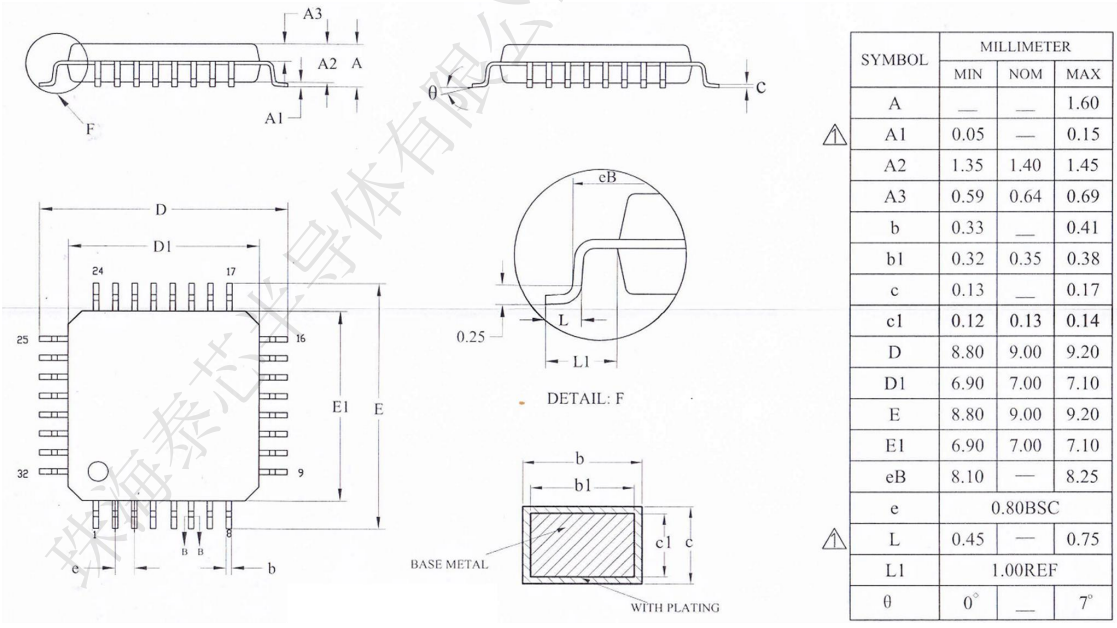
1.6.3. SSOP28



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.05	—	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.23	—	0.31
b1	0.22	0.25	0.28
c	0.20	—	0.24
c1	0.19	0.20	0.21
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	0.635BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05BSC		
θ	0°	—	8°

Figure 17 SSOP28 - package POD diagram

1.6.4. LQFP32



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.33	—	0.41
b1	0.32	0.35	0.38
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
eB	8.10	—	8.25
e	0.80BSC		
L	0.45	—	0.75
L1	1.00REF		
θ	0°	—	7°

Figure 18 LQFP32 - package POD diagram

2. Electrical Characteristics

2.1. Test conditions

All voltages are based on VSS/AVSS unless otherwise stated.

2.2. Minimum and maximum values

Unless otherwise specified, minimum and maximum values are tests performed at ambient temperature TA =-40 to 125 ° C and VCC =2 to 5.5 V.

2.3. Typical values

Typical values are based on TA = 27 ° C and VCC = 5V unless otherwise noted. These data are for design guidance only and have not been tested.

2.4. Typical curves

Unless otherwise noted, typical curves are intended for design guidance only and are not tested.

2.5. Load capacitance

The load conditions when measuring the pin parameters are shown in the figure below.

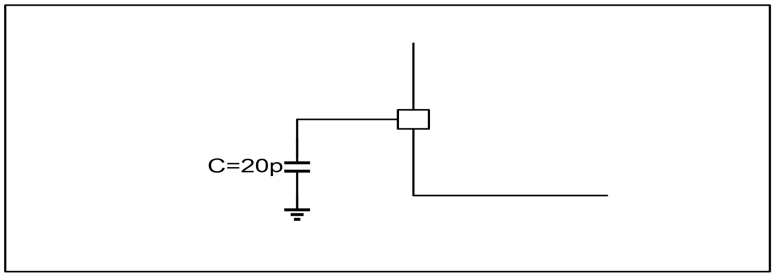


Figure 2-1 diagram of the load conditions for the pins

2.6. Pin input voltage

The way the input voltage on the pin is measured is shown in the figure below.

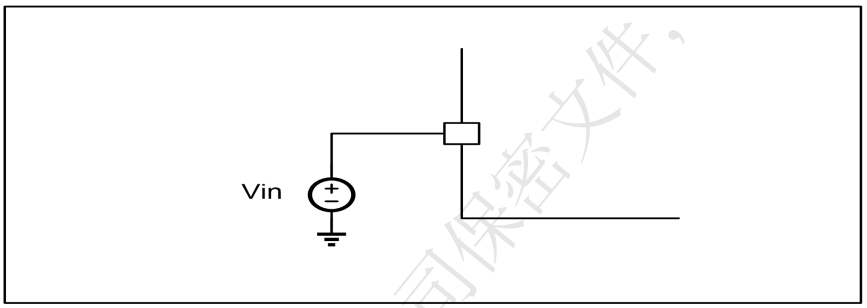


Figure 2-2 Input voltage diagram on the pin

2.7. Power supply Scheme

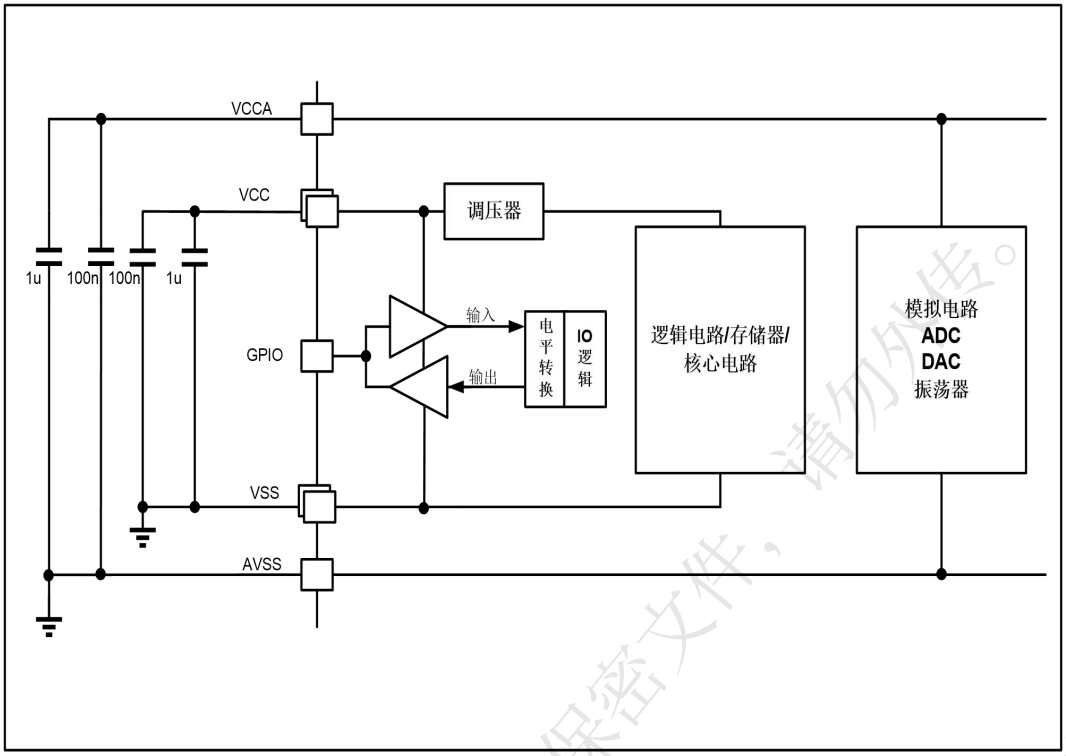


Figure 2-3 Power supply scheme (32Pin package condition)

2.8. Absolute maximum rating

A load applied to the device that exceeds the values given in the "Absolute Group Maximum Ratings" list (Tables 5, 6, 7) may cause the device to be permanently damaged. Only the maximum load that can be borne is given here and does not imply that the functional operation of the device under these conditions is correct. Long-term operation of the device under the maximum condition will affect the reliability of the device.

Table 2-1 Voltage characteristics

Symbols	Description	Minimum	Maximum	Units
VCC - VSS	External main supply voltage (includes AVCC and AVSS)(1)	0.3	5.5	V
VIN	Input voltage on 5V tolerated pins (2)	VSS - 0.3 -	5.5	V
	Input voltage on other pins (2)	VSS - 0.3 -	5.5	

|△VCCX|	Voltage difference between different supply pins	-	50	mV
|VSSX-VSS |	The voltage difference between the different ground pins	-	50	mV

1. All power (VCC, AVCC) and ground (VSS, AVSS) pins must always be connected to the external power supply system within allowable range.

2. The maximum value of the VIN must always be followed. See the table below for information on the maximum injection current values allowed.

Table 2-2 Current characteristics

Symbols	Description	Maximum	Units
IVCC	Total current through the VCC power cord (supply current)(1)	300	mA
IVCCA	Total current through the VCCA source line (supply current)(1)	20	mA
IVSS	Total current through the VSS ground wire (outgoing current)(1)	300	mA
IIO	Output feed current on any I/O and control pins	30	mA
	Output current on any I/O and control pins		

1, All main power (VCC, VCCA, and ground (VSS, AVSS) pins must always be connected to an external power supply to the extent permitted.

Table 2-3 Temperature characteristics

Symbols	Description	Maximum	Units
TSTG	Storage temperature range	-45 to 150	℃
TJ	Maximum junction temperature	125	℃

2.9. Working conditions

2.9.1. General working conditions

Table 2-4 General Working conditions

symbol	Parameters	Conditions	Minimum	Typical value	Maximum value	Units
f_{LIRC}	Internal low speed clock frequency	-	90K	128.3 K.	166K	Hz
f_{HIRC}	Internal high speed clock frequency	-	25.61 M	26M	26.39 M	
f_{OSC}	External clock frequency	-	1M	26M	32M	
V_{VCC}	Operating voltage	-	2.7	5	5.5	V
V_{VCCA}(1)	Simulate part of the operating voltage (ADC/DAC not used)	-	2.4	5	5.5	V

	Simulate part of the operating voltage (Use ADC/DAC)	-	2.7	5	5.5	
T_A	Ambient temperature:	-	- 40	-	105	℃

1, it is recommended to use the same power supply for and power supply, during power-on and normal operation, the maximum allowable difference between and 300mV;$VCCVCCAVCCVCCA$

2, if lower, as long as it does not exceed the higher value is allowed;$T_A T_J T_{J\max} P_D$

3, in the state of lower power consumption, as long as it is not exceeded, it can be extended to this range.$T_J T_{J\max} T_A$

2.9.2. Working conditions when power on and power off

All parameters given in the following table are tested under normal operating conditions.

Table 2-5 Operating conditions during power-on and power-off

Symbols	Parameters	Conditions	Minimum	Maximum	Units
t_{VCC}	V_{VCC}	T_A= 27 ℃	1000	-	Mu S
t_{VCCA}	V_{VCCA}		10	-	

2.9.3. Built-in reset and power control module features

All the parameters given in the following table are based on tests at ambient temperature and supply voltage listed in Table 12.VCC

Table 2-6 Built-in reset and power control module characteristics

Symbols	Parameters	Conditions	Minimum	Typical value	Maximum value	Units
VCC_{PVD}	Level selection for programmable voltage detector	LVDCON[8:4]=00000(rising edge)	-	2.094	-	v
		LVDCON[8:4]=00000(falling edge)	-	1.899	-	v
		LVDCON[8:4]=00001(rising edge)	-	2.095	-	v
		LVDCON[8:4]=00001(falling edge)	-	1.928	-	v
		LVDCON[8:4]=00010(rising edge)	-	2.055	-	v
		LVDCON[8:4]=00010(falling edge)	-	1.939	-	v
		LVDCON[8:4]=00011(rising edge)	-	2.148	-	v
		LVDCON[8:4]=00011(falling edge)	-	2.044	-	v
		LVDCON[8:4]=00100(rising edge)	-	2.257	-	v

		LVDCON[8:4]=00100(falling edge)	-	2.147	-	v
		LVDCON[8:4]=00101(rising edge)	-	2.357	-	v
		LVDCON[8:4]=00101(falling edge)	-	2.252	-	v
		LVDCON[8:4]=00110(rising edge)	-	2.462	-	v
		LVDCON[8:4]=00110(falling edge)	-	2.232	-	v
		LVDCON[8:4]=00111(rising edge)	-	2.566	-	v
		LVDCON[8:4]=00111(falling edge)	-	2.446	-	v
		LVDCON[8:4]=01000(rising edge)	-	2.769	-	v
		LVDCON[8:4]=01000(falling edge)	-	2.566	-	v
		LVDCON[8:4]=01001(rising edge)	-	2.903	-	v
		LVDCON[8:4]=01001(falling edge)	-	2.725	-	v
		LVDCON[8:4]=01010(rising edge)		3.060	-	v
		LVDCON[8:4]=01010(falling edge)		2.881	-	v
		LVDCON[8:4]=01011(rising edge)		3.211	-	v
		LVDCON[8:4]=01011(falling edge)		3.038	-	v
		LVDCON[8:4]=01100(rising edge)		3.373	-	v
		LVDCON[8:4]=01100(falling edge)		3.253	-	v
		LVDCON[8:4]=01101(rising edge)	-	3.534		v
		LVDCON[8:4]=01101(falling edge)	-	3.347		v
		LVDCON[8:4]=01110(rising edge)	-	3.670		v
		LVDCON[8:4]=01110(falling edge)	-	3.504		v
		LVDCON[8:4]=01111(rising edge)	-	3.835		v
		LVDCON[8:4]=01111(falling edge)	-	3.644		v
		LVDCON[8:4]=10000(rising edge)		3.664		v
		LVDCON[8:4]=10000(falling edge)		3.448		v
		LVDCON[8:4]=10001(rising edge)		3.867		v
		LVDCON[8:4]=10001(falling edge)		3.632		v
		LVDCON[8:4]=10010(rising edge)		4.071		v
		LVDCON[8:4]=10010(falling edge)		3.837		v
		LVDCON[8:4]=10011(rising edge)		4.279		v
		LVDCON[8:4]=10011(falling edge)		4.041		v
		LVDCON[8:4]=10100(rising edge)		4.481		v
		LVDCON[8:4]=10100(falling edge)		4.245		v
		LVDCON[8:4]=10101(rising edge)		4.692		v
		LVDCON[8:4]=10101(falling edge)		4.452		v
		LVDCON[8:4]=10110(rising edge)		4.894		v
		LVDCON[8:4]=10110(falling edge)		4.656		v
		LVDCON[8:4]=10111(rising edge)		5.088		v
		LVDCON[8:4]=10111(falling edge)		4.862		v
$V_{PVD\text{hyst}}$(2)	VCC hysteresis	-	104	180	239	mv
VDD_{PVD}	Level selection for programmabl	LVDCON[3:2]=00(rising edge)		1.05		
		LVDCON[3:2]=00(falling edge)		0.93		
		LVDCON[3:2]=01(rising edge)		1.15		
		LVDCON[3:2]=01(falling edge)		1.03		

	e voltage detector	LVDCON[3:2]=10(rising edge)		1.254		
		LVDCON[3:2]=10(falling edge)		1.138		
		LVDCON[3:2]=11(rising edge)		1.356		
		LVDCON[3:2]=11(falling edge)		1.243		
$V_{PVDhyst}$(2)	VDD lag	-	47	60	66	mv
$V_{POR/PDR}$	Power on/power off reset threshold	Falling Edge	-	0.65	-	v
		Rising edge	-	0.92	-	v
$V_{PDRhyst}$(2)	PDR lag	-	-	0.18	-	v
$V_{RSTTEMPO}$ (2)	Reset duration	-	-	3	-	ms

1, the characteristics of the product are guaranteed by design to the minimum value.$V_{POR/PDR}$

2, guaranteed by design, not tested in production.

Note: The reset duration is measured by charging (POR reset) to the moment when the user's application code reads the first instruction.

2.9.4. Power supply current Characteristics

Current consumption is a comprehensive indicator of a variety of parameters and factors, such as operating voltage, operating environment, I/O pin load, product software configuration, operating frequency, I/O pin turnover speed, program location in memory, and the code executed.

The current consumption measurements given in this section for all operating modes are executed in a compact and fairly high quality set of code.

The MCU is under the following conditions:

1, all I/O pins are in input mode and connected to a static level - or VSS(no load). VCC 2. All peripherals are turned off unless otherwise specified.

3, flash memory access time is adjusted to the frequency.f_{HCLK}

4, the command prefetch function is opened. When peripherals are turned on: =.$f_{HCLK}f_{PCLK1}$

2.9.5. External clock source features

High speed external user clock generated from an external oscillating source

The characteristic parameters given in the following table are measured using a high speed external clock source with ambient temperature and supply voltage conforming to common operating conditions.

Table 2-7 Characteristics of a high speed external subscriber clock

Symbols	Parameters	Conditions	Minimum value	Typical value	Maximum value	Units
f_{HSE_ext}	User external clock frequency		1	26	32	MHz
V_{HSEH}	XOSCI input pin high level voltage	-	-	746	-	mV
V_{HSHL}	XOSCO input pin low voltage	-	-	749	-	mV
$DuCy_{(HES)}$	Duty cycle	-	42	-	58	%
I_L	XOSCI input leakage current	-	-	-	0.5	uA
ACC_{HSE}	HSE accuracy	-	-	4	-	ppm
$t_{SU(HSE)}$	Starting time	-	-	2	10	ms

Guaranteed by design, not tested in production.

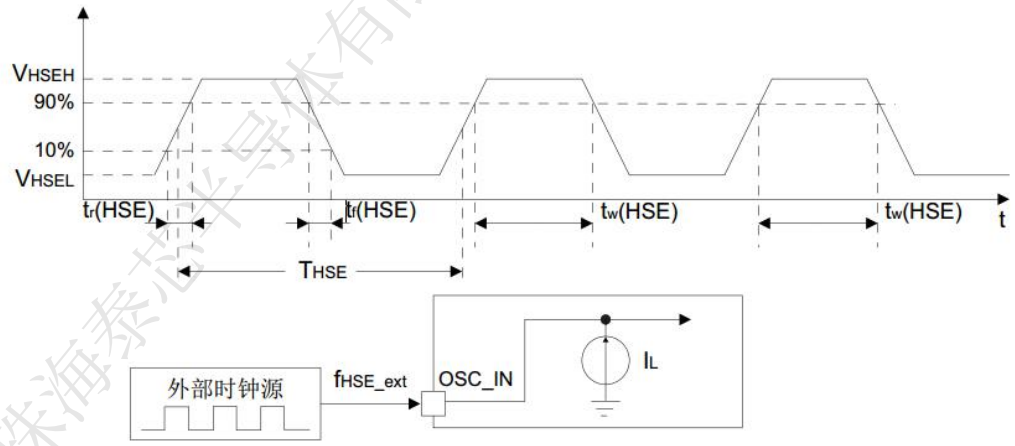


Figure 2-4 AC timing diagram of an external high speed clock source

Use a crystal oscillator/ceramic resonator to produce a high speed external clock

High Speed External Clock (HSE) A high speed external clock (HSE) can be

generated using an oscillator consisting of a 1 to 32MHz crystal/ceramic resonator. The information given in this section is based on a comprehensive characteristic evaluation using the typical external components listed in the table below. In the application, the resonator and load capacitor must be placed as close as possible to the pin of the oscillator to reduce output distortion and the stability time at startup. Consult the appropriate manufacturer for detailed parameters of the crystal resonator (frequency, package, accuracy, etc.).

1. The characteristic parameters of the resonator are given by the crystal/ceramic resonator manufacturer.

2, obtained by comprehensive evaluation, not tested in production.

3, for and, it is recommended to use high quality, designed for high frequency applications (typical value is) between 5pF to 25pF ceramic capacitor, and select the crystal or resonator that meets the requirements. $C_{L1}C_{L2}$Usually and have the same parameters. C_{L1}Crystal manufacturers usually give the parameters of the load capacitance in a serial combination of and. C_{L2}The capacitive reactance of the PCB and MCU pins should be taken into account when selecting and (the capacitance of the pins to the PCB board can be roughly estimated by 10pF).$C_{L1}C_{L2}$

4, relatively low RF resistance value, can provide protection to avoid problems caused by use in wet environments,

5, the leakage and bias conditions generated in this environment have changed. However, if the MCU is used in harsh wet conditions, the design needs to take this parameter into account.

6. $t_{SU(HSE)}$Startup time, measured from the beginning of HSE enablement in the software until a stable 26MHz oscillation is obtained. This value is measured on a standard crystal resonator, which may vary by crystal manufacturer

7. It varies widely.

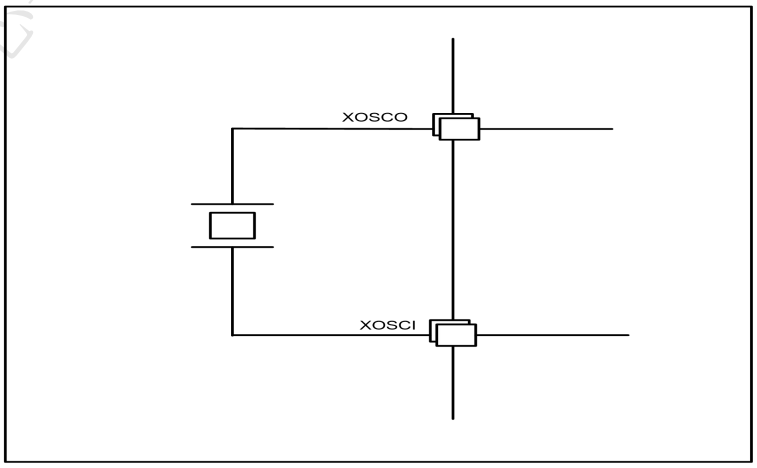


Figure 2-5 Typical applications using 26MHz crystals

2.9.6. Internal clock source characteristics

The characteristic parameters given in the following table are measured using ambient temperature and supply voltage conforming to common operating conditions.

High speed internal (HSI) oscillator

Table 2-8 HIS Oscillator characteristics

Symbols	Parameters	Conditions	Minimum value	Typical value	Maximum value	Units
V_{VCCA}	Supply voltage	-	2	5	5.5	V
f_{HRC}	Frequency	Test after trim at 25 ° C	25.9585	26	26.1167	MHz
ACC_{HSI} (3)	Accuracy of HSI oscillator	-40C to 125C	-	-	1.4	%
		-20C to 80C	-	-	0.71	
$t_{SU(HSI)}$	HSI oscillator startup time	-	-	60	-	us
$I_{VCCA(HSI)}$	HSI oscillator power consumption	Average power consumption	-	-	1.5	mA

1, V_{VCC}= 5V, TA = -40 ° C to 105 ° C, unless otherwise specified.
2, guaranteed by design, not tested in production.
3, the clock frequency accuracy is obtained by sampling measurement statistics.

Low speed internal (LSI) oscillator

Table 2-9 LSI oscillator characteristics

Symbols	Parameters	Conditions	Minimum	Typical value	Maximum value	Units
f_{LRC}	Frequency	TA=25℃	-	128.3	-	kHz
$t_{SU(LSI)}$	LSI oscillator startup time	-	-	-	10	us
$I_{DD(LSI)}$	LSI oscillator power consumption	-	-	2	4	uA

1, V_{AVCC}=5V, T A = -40 ° C to 105 ° C, unless otherwise specified.
2, obtained by comprehensive evaluation, not tested in production.
3, guaranteed by design, not tested in production.

2.9.7. Internal PLL characteristics

The characteristic parameters given in the following table are measured using ambient temperature and supply voltage conforming to common operating conditions.

Table 2-10 PLL features (built-in capless LDO for fractional frequency division)

Symbols	Parameters	Conditions	Minimum	Typical value	Maximum value	unit
V_{VCCA}	Supply voltage	-	2	5	5.5	V
Fckin	Enter frequency	-	1	26	32	MHz
Fckout	Output frequency	-	48	72		MHz
Ts	Stabilizing time			200	1000	us
TIE jitter@72M	Peak2Peak			150		ps
	RMS			10		ps
Current	Working current			850		uA

1, V_{VCC}= 5V, TA = -40 ° C to 105 ° C, unless otherwise specified.

2, guaranteed by design, not tested in production.

3, the clock frequency accuracy is obtained by sampling measurement statistics.

Table 2-11 Wake time from low power mode

Symbols	Parameters	Conditions	Maximum	Units
$t_{WUSLEEP}$	Wake up from sleep mode	Wake up from I/O	1.7	ms
t_{WUIDLE}	Wake up from idle mode	f=72MHz	13.8	ns
		f=128kHz	7.81	us
$t_{WUSTOPCLK}$	Wake up from stopclk mode	f=72MHz	13.8	ns
		f=128kHz	7.81	us

1. Wake up time is measured from the wake up event until the user program reads the first instruction.

2.9.8. Memory characteristic

Unless otherwise specified, all characteristic parameters are obtained at TA = -40 ℃ ~ 105 ℃.

Table 2-12 Flash memory characteristics

Symbols	Parameters	Conditions	Minimum	Typical value	Maximum value	Units
t_{prog}	Eight bits of programming time	-	6	-	7.5	us
t_{ERASE}	Page erase time	-	4	-	5	ms
t_{RC}	Read operation time	-	30	-	-	ns
t_{ME}	Whole chip erase time	-	20	-	40	ms
I_{DD}	Supply current	Read Mode	-	3	4.5	mA
		Write Pattern	-	-	3.5	mA
		Erase mode	-	-	2	mA

V_{prog}	Programming voltage	-	1.35	1.5	1.65	V

Table 2-13 Flash memory life and data retention period

Symbols	Parameters	Conditions	Minimum	Typical value	Maximum value	Units
NEND	Life span (number of erases)	-	-	20	-	Thousand times
t_{RET}	Data retention period	TA = 105℃	-	20	-	years
		TA = 25℃	-	100	-	

1. Obtained by comprehensive evaluation and not tested in production.
2, the cycle test is carried out in the whole temperature range.

2.9.9. EMC Characteristics

Sensitivity testing is sampled during the comprehensive evaluation of the product.

Functional EMS (Electromagnetic sensitivity)

When running a simple application (flashing 2 leds through the I/O port), two electromagnetic interferences are applied to the test sample until an error is produced, and the LED flicker indicates the creation of the error.

- Electrostatic discharge (ESD)(positive and negative discharge) is applied to all pins of the chip until a functional error is produced. This test complies with IEC1000-4-2 standards.
- FTB: A pulse swarm of transient voltages (forward and reverse) is applied through a 100 pF capacitor on VCC and VSS until a functional error is produced. This test complies with IEC1000-4-4 standards.

A chip reset allows the system to return to normal operation.

The test results are listed in the table below. This is a test based on the EMS level and type defined in the application notes.

Table 2-14 EMS features

Symbols	Parameters	Conditions	Level/type
V_{EFT}	Instantaneously varying pulse group voltage limits applied by 100pF capacitors on VCC and VSS that cause functional errors.		

Design robust software to avoid noise problems

The evaluation and optimization of EMC at the device level is performed in a typical application environment. It should be noted that good EMC performance is closely related to the user application and the specific software.

Therefore, it is recommended that users optimize their software for EMC and conduct certification tests related to EMC.

Software Recommendations

The flow of software must include the control of the program to run, such as:

1. Unexpected reset
2. Corrupted program counter
3, critical data is damaged (control registers, etc.)

In the ESD test, the voltage beyond the application requirements can be directly applied to the chip, when the unexpected action is detected, the software part needs to be strengthened to prevent the occurrence of irreversible errors.

2.9.10. Absolute maximum (electrical sensitivity)

Based on 2 different tests (ESD, Lath-Up), using specific measurement methods, the strength of the chip is tested to determine its strength

Performance in terms of electrical sensitivity.

Electrostatic Discharge (ESD)

Electrostatic discharge (a positive pulse followed by a negative pulse one second later) is applied to all pins of all samples, the size of the sample is related to the number of power supply pins on the chip (3 pieces x (n+1) power supply pins). This test complies with the JESD22-A114/C101 standard.

Static bolt lock

To evaluate latch performance, two complementary static latch tests were performed on six samples:

- For each power pin, provide a supply voltage that exceeds the limit.
- Inject current into each input, output, and configurable I/O pin.

This test complies with the EIA/JESD78A IC bolt-lock standard.

Table 2-15 ESD characteristics

Symbols	Parameters	Conditions	Maximum	Units
$V_{ESD(HBM)}$	Electrostatic discharge voltage (mannequin)	-	>6K	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charging device model)	-	>1K	V
I_{LU}	Static Latch class (Latch-up current)	@ 105 ℃	> + - 100	mA
		@ 25 ℃	> + - 150	

2.9.11. I/O port features

General input/output features

Unless otherwise specified, the parameters listed in the following table are measured according to the conditions in Table 9. All I/O ports are CMOS compatible. Support open drain output mode.

Table 2-16 Static I/O characteristics

Symbols	Parameters	Conditions	Minimum	Typical value	Maximum value	Units
V_{IL}	Input low-level voltage	-	-	2.099	-	V
V_{IH}	Enter a high level voltage	-	-	2.954	-	V
V_{hys}	I/O pin Schmidt trigger voltage hysteresis	-	-	0.855	-	V
I_{lkg}	Input leakage current	-	-	-	0.5	uA
R_{PU}	Pull up equivalent resistor	-	-	10.875	-	K Ω
R_{PD}	Pull down equivalent resistance	-	-	10.4	-	K Ω
C_{IO}	Capacitance of the I/O pin	-	1	1.5	2	pF

1, the hysteresis voltage of the switching level of the Schmidt trigger. Obtained by comprehensive evaluation, not tested in production.

2. If there is reverse current back in the adjacent pins, the leakage current may be higher than the maximum value.

3, pull-up and pull-down resistors are designed as a true resistor in series

with a switchable PMOS/NMOS implementation. The resistance of this PMOS/NMOS switch is very small (about 10%).

All I/O ports are CMOS-compatible (no software configuration required) and their features take into account most rigorous CMOS processes.

Output Drive Current

GPIO (Universal input/Output Port) can absorb or output up to ±30mA of current.

In user applications, the number of I/O pins must ensure that the drive current does not exceed the absolute maximum rating given in section 5.2:

- The sum of the current drawn from all I/O ports, plus the maximum operating current drawn by the MCU on the VCC, must not exceed the absolute maximum rating.I_{VCC}
- The sum of the current absorbed by all I/O ports and flowing out of the VCC, plus the maximum operating current drawn by the MCU on the VCC, cannot exceed the absolute maximum rating.$V_{SS}V_{SS}I_{VSS}$

Table 2-17 IOL/IOH characteristics

IO Type	Mode	Symbols	Configuration	Minimum value	Typical value	Maximum value	Units
GPIO	Nomal Mode	IoH	00	-	1.18	-	mA
			01	-	21.15	-	mA
			10	-	39.3	-	mA
			11	-	65.6	-	mA
	Nomal Mode	IoL	00	-	1.24	-	mA
			01	-	22.33	-	mA
			10	-	42.1	-	mA
			11	-	97.4	-	mA

1, GPIO method of measuring IOL/IOH, external resistor pull-up power supply/pull-down to ground, measure the current on the resistor when the voltage on I/O is 1/2*VCC

Input/output AC characteristics

The definitions and values of the I/O AC characteristics are given in Figure 15 and Table 30 respectively.

Unless otherwise specified, the parameters listed in Table 30 are measured using ambient temperature and supply voltage conforming to the conditions in Table 9.

Table 2-18 Input/output AC features

IO Type	Configuration (drive)	Symbol	Parameters	Minimum value	Typical value	Maximum value	Units
GPIO (loaded 20p capacitor)		$f_{max(IO)out}$	Maximum frequency	-	26M	-	Hz
	00	$t_{f(IO)out}$	Descent time	-	128	-	ns
	00	$t_{r(IO)out}$	Rise time	-	146	-	ns
	01	$t_{f(IO)out}$	Descent time	-	7.6	-	ns
	01	$t_{r(IO)out}$	Rise time	-	8	-	ns
	10	$t_{f(IO)out}$	Descent time	-	4.6	-	ns
	10	$t_{r(IO)out}$	Rise time	-	5	-	ns
	11	$t_{f(IO)out}$	Descent time	-	3.4	-	ns
	11	$t_{r(IO)out}$	Rise time	-	4.2	-	Ns

1. The speed of the I/O port can be configured with GPIOx_OSPEEDL. See the instructions for GPIO port Configuration Registers in this chip reference manual.

2. The maximum frequency is defined in Figure 15.

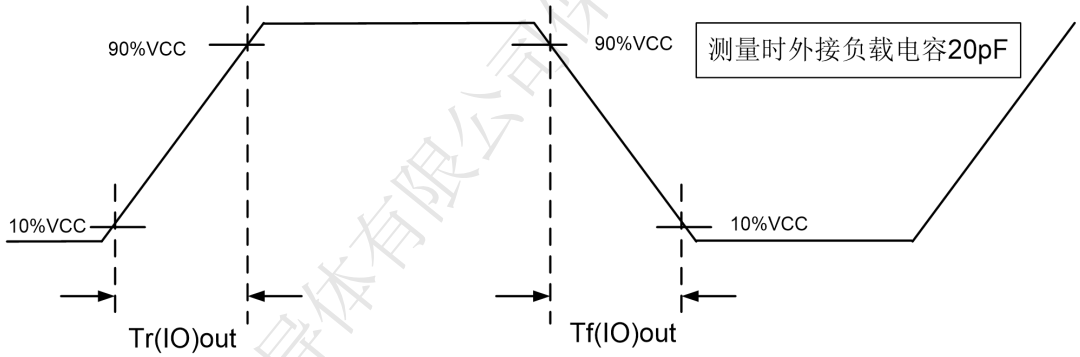


Figure 2-6 I/O AC characteristic definition

2.9.12. Timer Characteristics

The parameters listed in the table below are guaranteed by design

See section 5.3.10 for details on the features of input/output multiplexing function pins (output comparison, input capture, external clock, PWM output)

Table 2-19 TIMx[1] features

Symbols	Parameters	Conditions	Minimum	Maximum	Units
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
$t_{res(TIM)}$	Timer resolution time	$f_{TIMxCLK} = 72MHz$	13.8	-	ns

Res_{TIM}	Timer resolution	-	-	16	position
$t_{COUNTER}$	16-bit counter clock cycle when internal clock is selected	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK} = 72MHz$	0.0138	1260	us
t_{MAX_COUNT}	Maximum possible count	-	-	65536 x 128	$t_{TIMxCLK}$
		$f_{TIMxCLK} = 72MHz$	-	115.76	ms

1, TIMx is a generic name that stands for timer0/1/2/3/4 4/5.

2.9.13. Communication interface

I2C bus

Unless otherwise specified, the parameters listed in the following table are measured using ambient temperature, frequency, and VCC supply voltage conforming to the conditions in Table 12. f_{PCLK1}The I2C interface complies with the standard I2C communication protocol with the following limitations: SDA and SCL are not 'true' pins, and when configured to open leaky outputs, the PMOS tube between the lead-out pin and the VCC is turned off, but still present. I2C interface characteristics are listed in the following table, see section 5.3.10 for details on the characteristics of input/output multiplexing function pins (SDA and SCL).

Table 2-20 I2C interface characteristics

Symbols	Parameters	Standard I2C		Fast I2C		unit
		Minimum	Maximum	Minimum	Maximum	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	us
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	us
$t_{su(SDA)}$	SDA establishment time	250	-	100	-	us
$t_{h(SDA)}$	SDA data hold time	0	-	0	900	ns
$t_{r(SDA)}t_{r(SDL)}$	SDA and SCL rise time	-	1000	$2.0 + 0.1C_b$	300	
$t_{f(SDA)}t_{f(SDL)}$	SDA and SCL drop time	-	300	-	300	
$t_{h(STA)}$	Start condition hold time	4.0	-	0.6	-	us
$t_{su(STA)}$	Repeated starting conditions establish time	4.7	-	0.6	-	
$t_{su(STO)}$	Stop condition build time	4.0	-	0.6	-	
$t_{w(STO:STA)}$	Time from stop condition to	4.7	-	1.3	-	

	start condition (bus idle)					
C_b	Capacitive load per bus		400		400	pF

1, guaranteed by design, not tested in production.

2, in order to achieve the maximum frequency of the standard mode I2C, fPCLK1 must be greater than 3MHz. To achieve the maximum frequency of fast mode I2C, fPCLK1 must be greater than 12MHz.

3, if it is not required to lengthen the low level time of the SCL signal, only the maximum holding time of the starting condition needs to be met.

4. In order to cross the undefined area of the SCL falling edge, at least 300nS must be guaranteed on the SDA signal inside the MCU

5, the holding time.

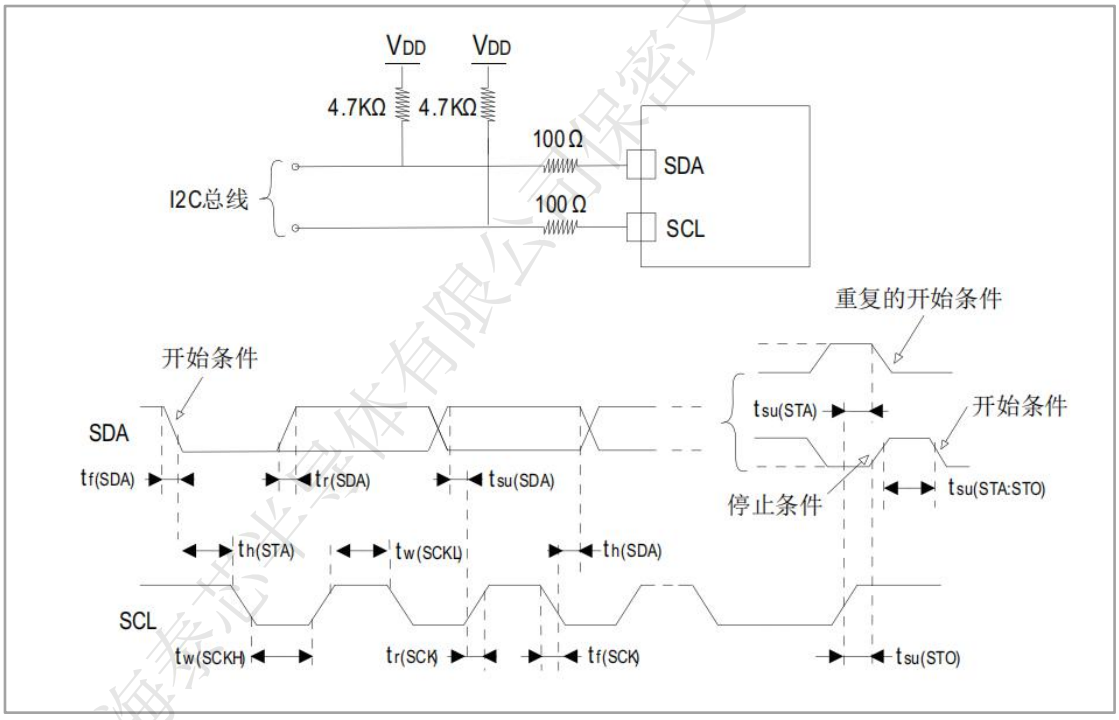


Figure 2-7 I2C bus AC waveform and measurement circuit

The measuring points are set at CMOS levels: 0.3VCC and 0.7VCC.

SPI interface characteristics

Unless otherwise specified, the parameters listed in the following table are measured using ambient temperature, frequency and VCC supply voltage conforming to

the conditions in Table 8. f_{PCLK}

See section 5.3.10 for details on the characteristics of input/output multiplexing function pins (NSS, SCK, MOSI, MISO).

Table 2-21 SPI features

Symbols	Parameters	Conditions	Minimum	Maximum	unit
$f_{SCK}1/t_{c(SCK)}$	SPI clock frequency	Master Mode	0	26	MHz
		Slave Mode	0	13	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Load capacitance: C=30pF	-	8	ns
$t_{su(NSS)}$ (2)	NSS establishment time	From Mode	$4t_{PCLK}$	-	ns
$t_{h\ (NSS)}$ (2)	NSS hold time	From Mode	73	-	ns
$t_{w(SCKH)}$ (2) $t_{w(SCKL)}$ (2)	SCK high and low times	Master mode, $4f_{PCLK} = 26MHz$	50	60	ns
$t_{su(SI)}$ (2)	Data entry build time, from pattern	-	1	-	ns
$t_{h\ (SI)}$ (2)	Data entry hold time, from mode	-	3	-	ns
$t_{a(SO)}$ (2)(3)	Data output access time	From mode, $f_{PCLK} = 26MHz$	0	77	ns
		From pattern, $f_{PCLK} = 24MHz$	-	$4t_{PCLK}$	ns
$t_{dis(SO)}$ (2)	Data output disable time	Slave Mode	10	-	ns
$t_{v(SO)}$ (2)(1)	Data output valid time	From mode (after enable edge)	-	25	ns
$t_{v(MO)}$ (2)(1)		Master mode (after enable edge)	-	3	ns
$t_{h\ (SO)}$ (2)	Data output hold time	From mode (after enable edge)	25	-	ns
$t_{h\ (MO)}$ (2)		Master mode (after enable edge)	4	-	ns

1, derived from comprehensive evaluation, not tested in production.

2, the minimum value indicates the minimum time to drive the output, the maximum value indicates the maximum time to get the data correctly.

3, the minimum value indicates the minimum time to turn off the output, the maximum value indicates the maximum time to put the data line in a high resistance state.

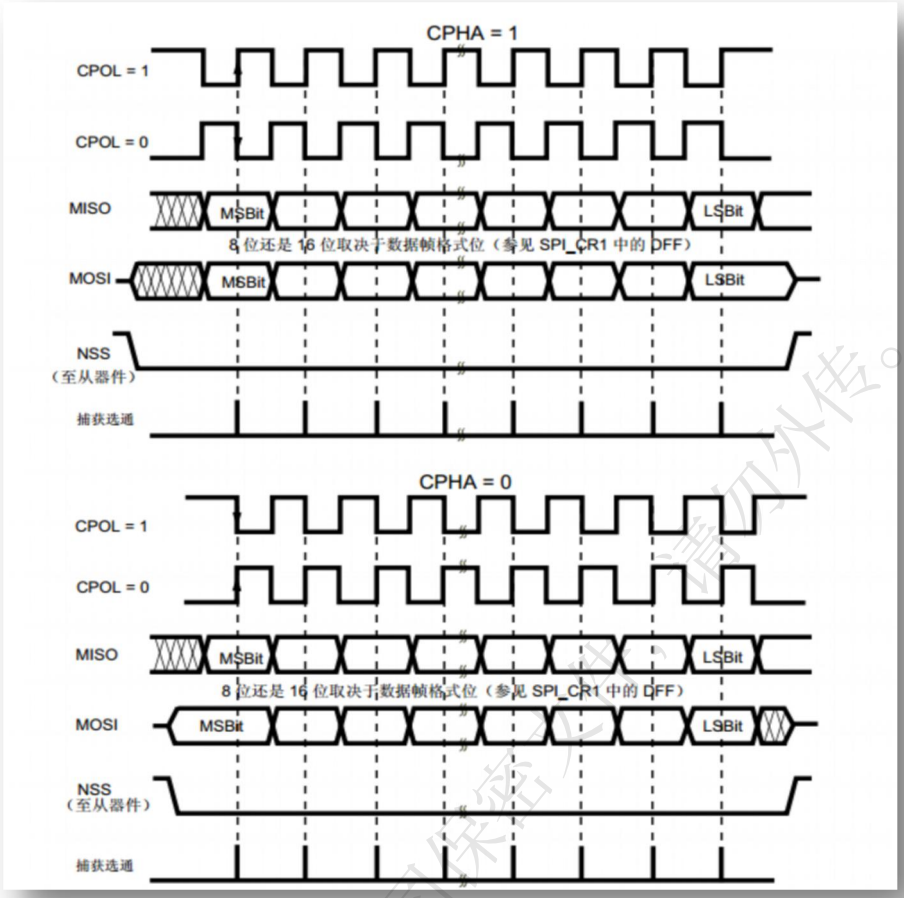


Figure 2-8 SPI timing diagram

The measuring points are set at CMOS levels: 0.3VCC and 0.7VCC.

2.9.14. 12-bit ADC characteristics

Unless otherwise specified, the parameters in the following table are measured using ambient temperature, frequency, and supply voltage as specified in Table 12. $f_{PCLK2} V_{DDA}$

Note: It is recommended to perform one calibration each time you power on.

Table 2-22 ADC characteristics

symbol	Parameters	Conditions	Minimum	Typical value	Maximum value	Units
V_{VCCA}	Supply voltage	-	2	5	5.5	V
$I_{VCCA}{}^{(1)}$	Current consumption	-	-	1	-	mA
f_{ADC}	ADC Clock Frequency	-	-	-	26	MHz

Fconv	Conversion Rate	-	-	-	1.3	MHz
V_{AIN}(2)	Conversion voltage range	-	0	-	VCCA	V
R_{AIN}(2)	External input impedance	-	-	1.5	-	Kohm
C_{ADC}(2)	Internal sampling and holding capacitance	-	-	1.28	-	pF
t_{STAB}(2)	Power-on time	-	-	-	1100	us
t_{conv}(2)	Total conversion time	-	-	5 * 1 /f_{ADC}	-	us
V_{AIN}(2)	Switching voltage range	-	0	-	VCCA	V
Enob				10		Bit

1, guaranteed by comprehensive evaluation, not tested in production.

2. Guaranteed by design, not tested in production.

3. In this series, the ADC reference voltage is internally connected to the VCCA.

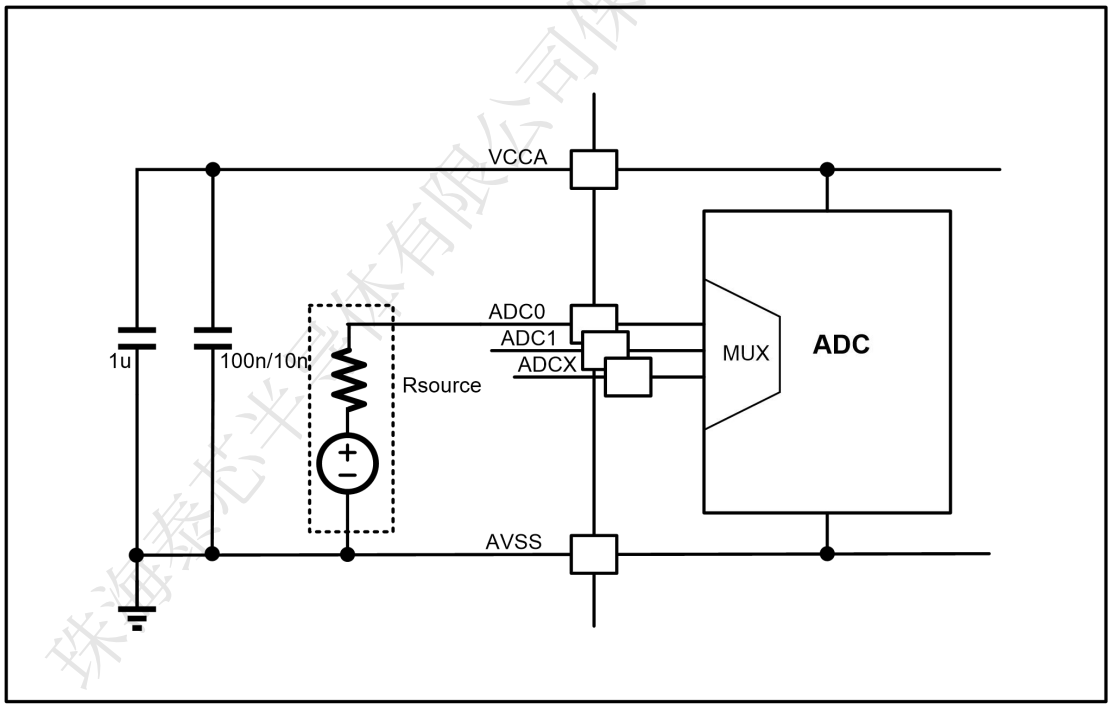


Figure 2-9 A typical connection diagram using an ADC

1. For the values of, and, see Table 37. $R_{AIN}R_{ADC}C_{ADC}$

$2C_{parasitic}$, indicating that the PCB (related to welding and PCB layout quality) and the parasitic capacitance on the pad (about 7pF) of the larger value will reduce

the accuracy of the conversion, the solution is to reduce$C_{\text{parasitic}}f_{ADC}$

PCB design recommendations

The decoupling of the power supply must be connected according to the figure below. The 10 nF capacitors in the figure must be porcelain dielectric capacity (good quality) and they should be as close to the MCU chip as possible.

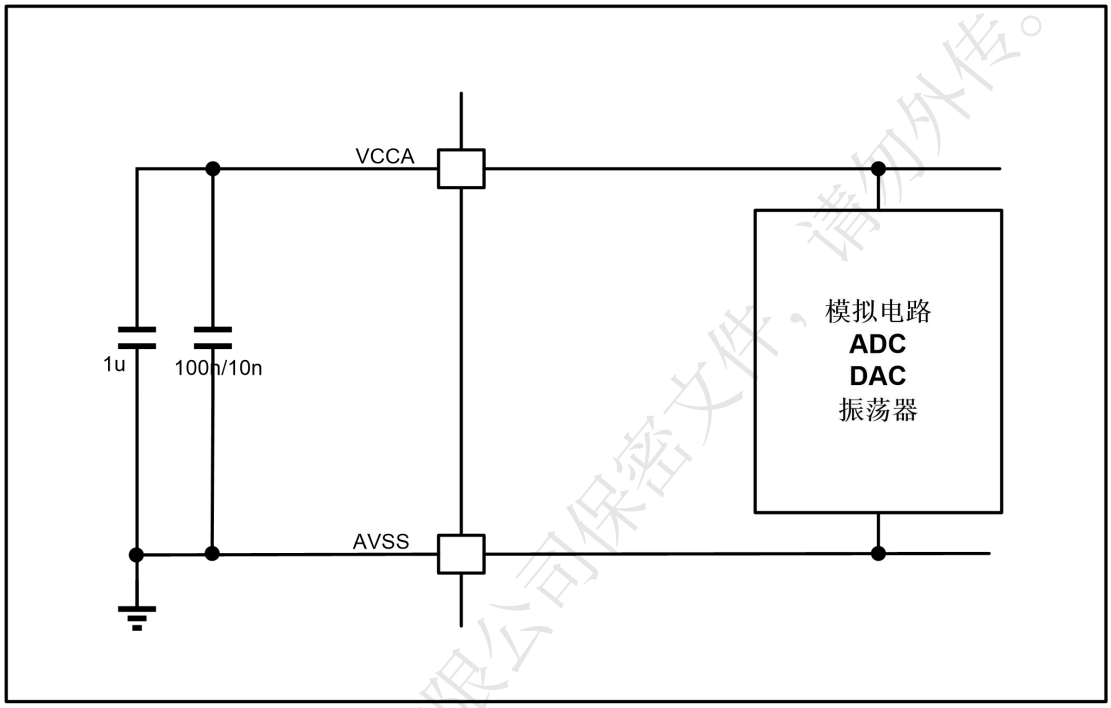


Figure 2-10 Power supply and reference power supply decoupling lines

2.9.15. Temperature sensor characteristics

Table 2-23 Temperature sensor characteristics

Symbols	Parameters	Conditions	Minimum	Typical value	Maximum value	Units
T_L(1)	Average slope	TA=0~90℃	3.683	3.9	4.117	mV/℃
		TA=-40~125℃	3.443	3.9	4.357	mV/℃
V_{25}(1)	Voltage at 25 ° C	-	-	1.16	-	V
t_{start}(2)	Build up time	-	-	-	5	us
$T_{\text{s\_temp}}$(2)	ADC sampling time when reading temperature	-	5	-	-	us

1, guaranteed by comprehensive evaluation, not tested in production.

2. Guaranteed by design, not tested in production.

3, the shortest sampling time can be determined by the application through many cycles.

$4V_{VCC}$, ==5V.V_{VCCA}

2.9.16. 5 bit DAC feature

Table 2-24 5bitDAC features

Symbols	Parameters	Conditions	Minimum	Typical value	Maximum value	Units
V_{VCCA}	Analog supply voltage	-	2	5	5.5	V
I_{VCCA}(1)	Current consumption	-	-	15	-	uA
C_L	Capacitive load	-	-	1.5	-	pF
R_0	Output impedance	-	10.35		82.875	Kohm
V_{DAC_OUT}	Voltage output	-	0	-	VCCA	V
DNL(1)	Nonlinear error	-	-	-	0.26	LSB
INL(1)	Linear error	-	-	-	0.09	LSB
Offset(1)	Coding Offset error (ox20)	-	-	-	- 17	mV

1, guaranteed by comprehensive evaluation, not tested in production.

2.9.17. 8 bit DAC features

Table 2-25 8bitDAC features

Symbols	Parameters	Conditions	Minimum	Typical value	Maximum value	Units
V_{VCCA}	Analog supply voltage	-	2	5	5	V
I_{VCCA}(1)	Current consumption	-	-	40	-	mA
C_L	Capacitive load	-	-	1.5	-	pF

R_0	Output impedance	-	10.35		82.875	Kohm
V_{DAC_OUT}	Voltage output	-	0	-	4.8	V
DNL(1)	Nonlinear error	-	-	-	1.04	LSB
INL(1)	Linear error	-	-	-	0.94	LSB
Offset(1)	Encoding offset error 0x800	-	-	-	7.9	mV

1, guaranteed by comprehensive evaluation, not tested in production.

2, VCC=VCCA.

2.9.18. Comparator characteristics

Table 2-26 Comparator features

Symbols	argument	Register configuration	Minimum	Typical value	Maximum value	Units
V_{VCCA}	Analog supply voltage	-	2	5	5.5	V
OFFSET	Offset voltage	-	7.21	2.57	12.35	mV
DELAY(1)	Propagation delay	-	-	60	-	ns
I_q(2)	Mean operating current	-	-	14.8	-	uA

1, the time difference between the output flip 50% and the input flip.

2, the total consumption current average, working current.

2.9.19. Operational amplifier characteristics

Table 2-27 Built-in operational amp features

Symbols	Parameters	Conditions	Minimum	Typical value	Maximum value	Units
V_{VCCA}	Analog supply voltage	-	2	5	5.5	V
V_{IN}	Input voltage	-	0	-	VCCA - 1.2 -	V

V_{OUT}	Output voltage	-	0.3	-	VCCA - 0.3 -	V
I_{VCCA}(1)	Current consumption	-	-	0.56	-	mA
R_L	Load impedance	$V_{OUT}=\max V_{AVCC}=5$	40	-	-	Kohm
		V_{AVCC}-$V_{OUT}>0.7$	15	-	-	Kohm
		V_{AVCC}-$V_{OUT}>1.2$	5	-	-	Kohm
V_{offset}	Input offset voltage	-	-	-	5.4	mV
T_{start}	Initialization time	Power on to adjust offset voltage	13.5	-	-	ms
SR	Output voltage swing rate	$R_L=25K$ $C_L=5pF$	-	13	-	V/us
PM	Phase margin		-	60	-	Deg
GM	Gain margin		-	40	-	dB
UGBW	Unit-gain bandwidth		-	16	-	MHz
GAIN	Loop gain	$R_L=25K$ $V_{AVCC}-V_{OUT}>0.3$ $V_{AVCC}=5$	-	80	-	dB

1, guaranteed by comprehensive evaluation, not tested in production.